PCA8802

Smartcard RTC; ultra low power oscillator with integrated counter for initiating one time password generation

Rev. 3 — 30 March 2012 Product data sheet

1. General description

The PCA8802 is a CMOS integrated circuit for battery operation, typically supplied by button cells or flexible polymer batteries. Incorporated is a 32.768 kHz quartz crystal oscillator circuit including the two load capacitors. The circuit is optimized for a quartz with 6 pF load capacitance specification. Higher values can also be used with the addition of external load capacitors.

The main function of the oscillator is to generate a $\frac{1}{32}$ Hz clock signal which is used to increment a 24 bit binary counter. The counter can be read over the serial interface and may also be set to any desired value. Control over the divider chain also allows for accurate starting of the counter. Incrementing of the counter value during read is prevented by freezing of the counter during access.

An interrupt signal is also available and is triggered coincident with the counter updating. This signal may be used as a wake-up for a microcontroller.

2. Features and benefits

- 32.768 kHz quartz oscillator, amplitude regulated with excellent frequency stability and high immunity to leakage currents
- Very low current consumption: typically 130 nA
- Two wire serial interface (I^2C-bus)
- Integrated 24 bit counter with auto increment every 32 seconds
- Interrupt output for processor wake-up
- Stop function for accurate time setting and current saving during shelf life
- User test modes for accelerated application testing and development
- Two integrated quartz crystal oscillator capacitors

3. Applications

- One time password function generators
- Ultra low power time keeper circuit

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Name	Description	Delivery form	Version
PCA8802CX8/B/1	PCA8802CX	WLCSP8; wafer level chip-size package; 8 bumps; 1.19 × 1.14 × 0.29 mm	chip with solder bumps in tape and reel	PCA8802CX
PCA8802U/2AA/1	PCA8802U	WLCSP8; wafer level chip-size package; 8 bumps; 1.19 × 1.14 × 0.22 mm	chip with gold bumps in tray	PCA8802U
PCA8802U/12AA/1	PCA8802U	WLCSP8; wafer level chip-size package; 8 bumps; 1.19 × 1.14 × 0.22 mm	sawn 6-inch wafer with chips with gold bumps on Film Frame Carrier (FFC) for 8-inch wafer	PCA8802U

5. Marking

Table 2. Marking codes

Type number	Marking code
PCA8802CX8/B/1	PC8802-1
PCA8802U/2AA/1	PC8802-1
PCA8802U/12AA/1	PC8802-1

6. Block diagram

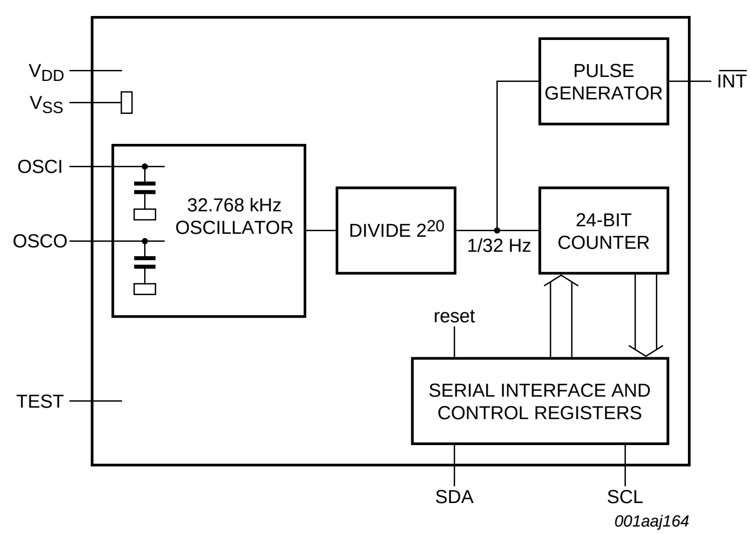
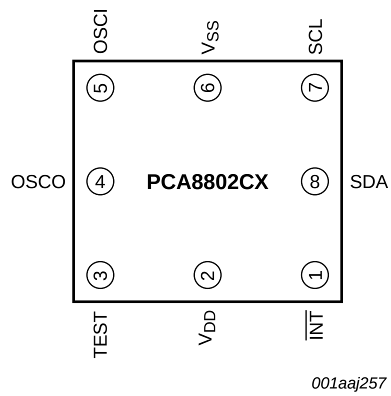


Fig 1. Block diagram

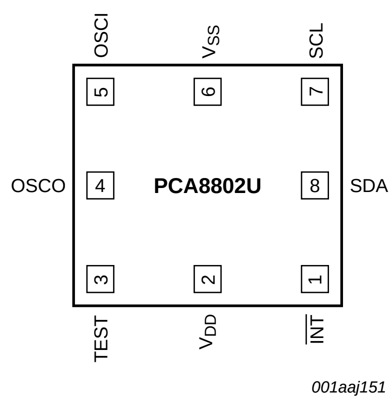
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 30.

Fig 2. Pinning diagram of PCA8802CX



Top view. For mechanical details, see Figure 31.

Fig 3. Pinning diagram of PCA8802U

7.2 Pin description

Table 3. Pin description for PCA8802

Symbol	Pin	Description
$\overline{\text{INT}}$	1	interrupt and test mode output, push-pull
V_{DD}	2	supply voltage
TEST	3	test pin; must be connected to V_{SS}
OSCO	4	oscillator output
OSCI	5	oscillator input
V_{SS}	6	ground
SCL	7	serial interface, clock
SDA	8	serial interface, bidirectional data line; push-pull

8. Device protection diagram

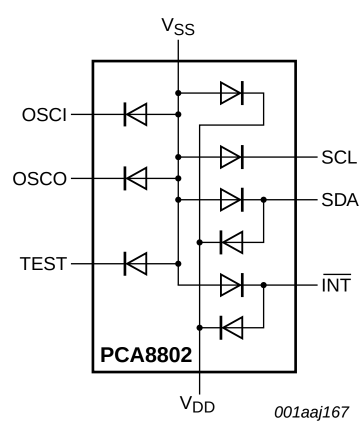


Fig 4. Diode protection diagram

9. Functional description

The PCA8802 is an ultra low power device for battery operations. The integrated oscillator circuit generates a $\frac{1}{32}$ Hz clock signal to increment a 24 bit counter. The communication between the PCA8802 and other devices is made via an I^2C-bus.

The device is always running but for longer storage time it can be switched off and on again in case of delivery.

The functions of the device can be controlled with the following instruction set:

Table 4. Instruction set overview

Instruction	Description	Reference
wrt_cmd	device write access	Section 9.6.2
dvs_cmd	divider start or stop switch	Section 9.6.3
pwd_cmd	low power mode switch	Section 9.6.4
32k_cmd	32.768 kHz clock signal on the pin $\overline{\text{INT}}$ switch	Section 9.6.5
fst_cmd	fast system development mode switch	Section 9.6.6
set_cmd	set counter instruction	Section 9.6.7
rd_cmd	counter read instruction	Section 9.6.8

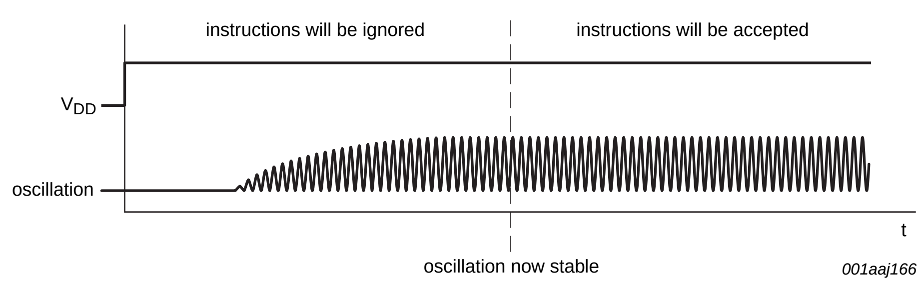
9.1 Oscillator

The 32.768 kHz oscillator includes two integrated load capacitors and an automatic gain control to ensure a reliable start-up.

For prototype development and system debugging, it is possible to output a 32.768 kHz square wave on the $\overline{\text{INT}}$ pin with the 32k_cmd instruction.

9.1.1 Power-on

At initial power-on, when the oscillator has not yet started, a reset will be generated. During this state the serial interface will not respond when accessed. To ensure that the oscillator has started and the serial interface is accessible, it is recommended that the master attempts to make write-read accesses to the counter register.



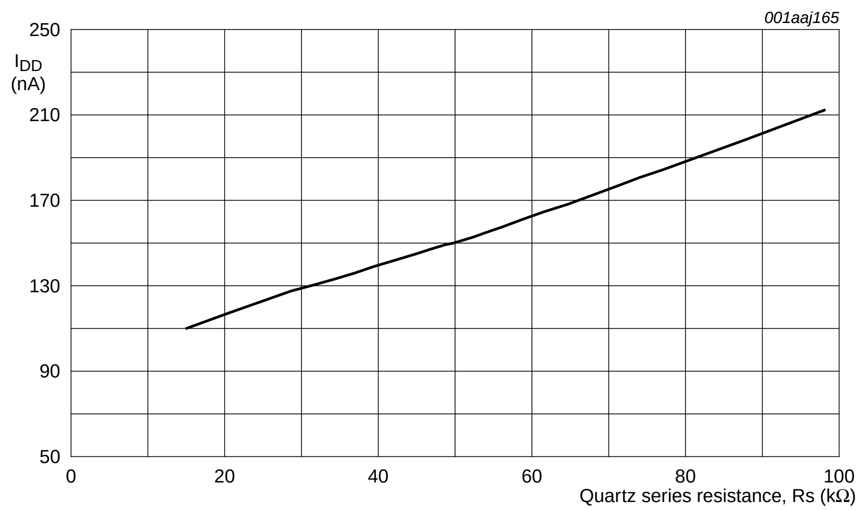
Exit from Power-down mode will give the same behavior as start-up.

Fig 5. Power-on reset

9.1.2 Low power operation

With the power-down instruction (pwd_cmd) the oscillator can be stopped and the device can be put into a low power state where power consumption is reduced to an absolute minimum. The chip would normally reset when the oscillator is stopped, so to prevent a reset of the chip during this state, a special software power-down sequence must be used (see Table 7). In power-down state, the interface is still accessible.

A prime consideration for low power consumption is the series resistance R_s of the quartz used. The series resistance acts as a loss element. Low R_s will reduce current consumption further.



V_{DD} = 3 V.

Fig 6. I_{DD} with respect to R_s

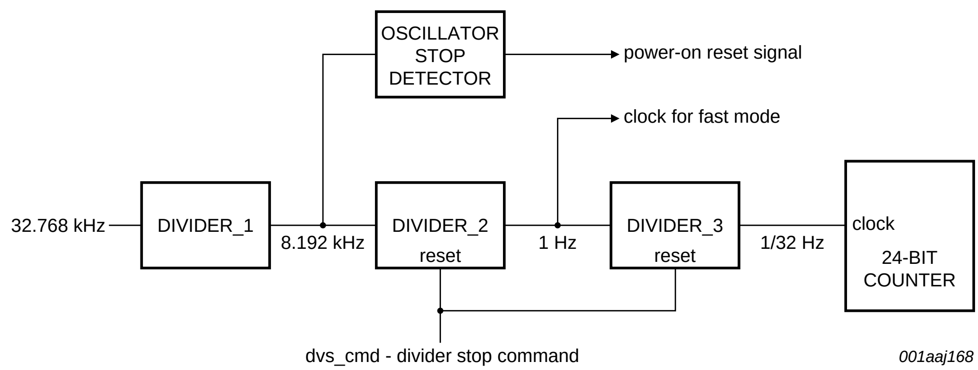
9.2 Divider

The divider chain is responsible for reducing the 32.768 kHz oscillator frequency down to $\frac{1}{32}$ Hz.

The dividers (see Figure 7) divider_2 and divider_3 may be reset with the dvs_cmd instruction. The 24 bit counter may be set when the dividers are held in reset, but this is not a requirement. This allows for accurate setting and restarting of the counter.

The interface is asynchronous to the quartz oscillator and the state of divider_1 can not be known when the dvs_cmd is enabled. The 8.192 kHz clock could have just occurred and hence a delay of $\frac{1}{8192}$ seconds will occur before the next increment of the divider_2, or the 8.192 kHz clock could be just about to occur and immediately increment the divider_2.

As a consequence, an uncertainty of between zero and one 8192 Hz clock period (i.e. a time uncertainty of about 0 s to 122 μs) will be present when restarting the counter.



Divider_1 = dividing by 4.

Divider_2 = dividing by 8192.

Divider_3 = dividing by 32.

Fig 7. Divider chain

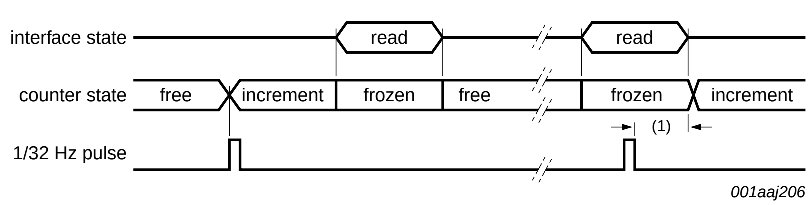
9.3 Binary counter

A 24 bit binary roll over counter is implemented. The counter is reset at power-on.

The counter can be set to any value using the set_cmd instruction. The set_cmd instruction allows partial writing of data. Partial writing of the data parameters will result in partial setting of the counter, e.g. if data transfer is stopped after P1[23:16] (see Table 5) is transmitted, then only bit 23 to bit 16 will be updated. The counter will not increment whilst being set.

The counter can be halted by means of stopping the dividers using the dvs_cmd instruction.

The counter can be read at any time and the counter value will remain stable during reading. If the counter is due to increment during the read or write cycle, then the request to increment will be held off until after the read has concluded. For this reason it is important to read the counter in bursts, ensuring that an interface STOP condition (see Section 9.5.4) is present between read accesses. Reading for periods of more then 32 seconds at a time will result in loss of counts.



(1) Increment delayed until after the read has finished.

Fig 8. Counter behavior during read access

9.4 Pulse generator

An interrupt pulse is available at the $\overline{\text{INT}}$ pin. This pulse is generated once every 32 seconds and could be used to wake up a microcontroller to perform a periodic function e.g. to calculate and update an LCD display with a new one-time password.

A pulse is generated coincident with the increment of the counter. The new counter value will be available immediately.

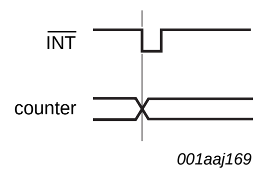


Fig 9. Pulse generator

9.5 I²C-bus interface

9.5.1 Interface protocol

The serial interface is based on the I²C-bus protocol. The I²C-bus protocol has the advantage of being robust in terms of immunity to electrical noise. Although the PCA8802 does not have the signal filters inside the interface pins, the slave address and acknowledge hand shaking is nevertheless implemented.

For power saving, the SDA output is push-pull instead of the more traditional open-drain output. Push-pull prevents the need for power consuming pull-up resistors, but does limit the operation to point to point only.

The following slave addresses plus a write and read bit are reserved for the PCA8802:

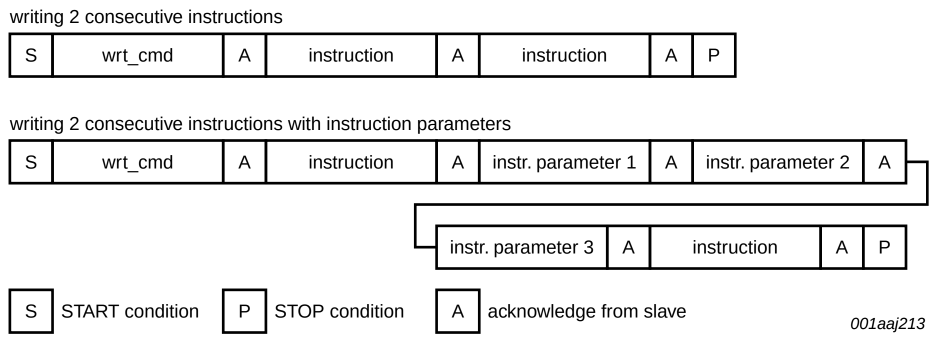
- write: 1010 0000
- read: 1010 0001

An incorrect slave address will result in the device ignoring all bus data. A STOP or START condition (see Section 9.5.4) will be required before a new transfer can be made.

9.5.1.1 The writing protocol

The writing protocol is shown in Figure 10.

There is no restriction for the order of sending instructions. As many instructions as needed may be sent in one access. The total duration of one access must not exceed 32 seconds (see Figure 12).

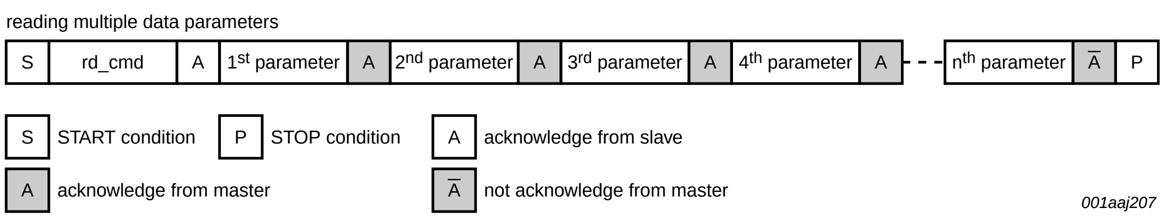


Wrt_cmd is slave address plus write bit.

Fig 10. Writing protocol

9.5.1.2 The reading protocol

The reading protocol is shown in Figure 11.

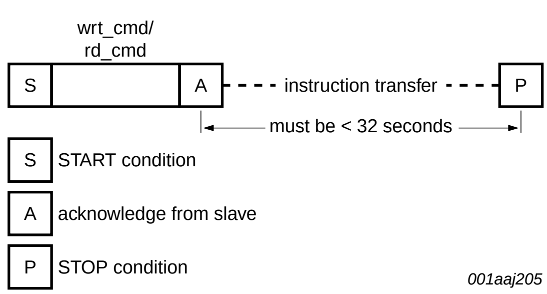


Rd_cmd is slave address plus read bit.

Fig 11. Reading protocol

9.5.1.3 Reading and writing limitations

As the counter is frozen during interface accesses, all access must be completed within 32 seconds (see Figure 12). If this rule is not adhered to, then counts will be dropped.



Wrt_cmd is slave address plus write bit.

Rd_cmd is slave address plus read bit.

Fig 12. Access restrictions

9.5.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is shown in Figure 13.

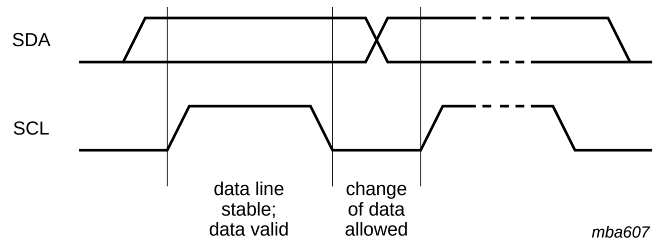


Fig 13. Bit transfer

9.5.3 Bit order

Data is transferred MSB first.

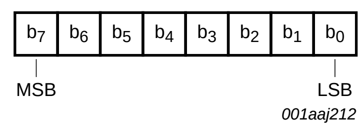


Fig 14. Bit transfer

9.5.4 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are shown in Figure 15.

The data on SDA is sampled with the rising edge of SCL. Data is output to SDA on the falling edge of SCL.

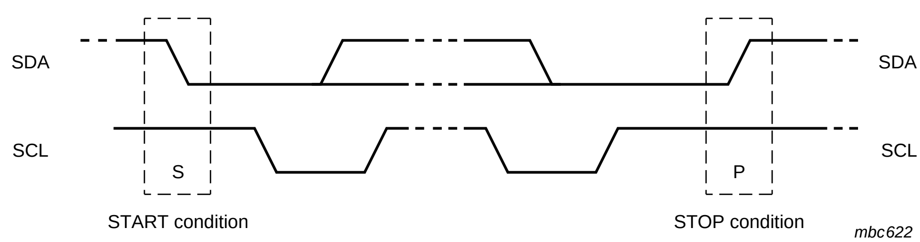


Fig 15. Definition of START and STOP conditions

9.5.5 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the device which is controlled by the master is the slave.

9.5.6 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited, but the duration of the access must not exceed 32 seconds. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement is shown in Figure 16.

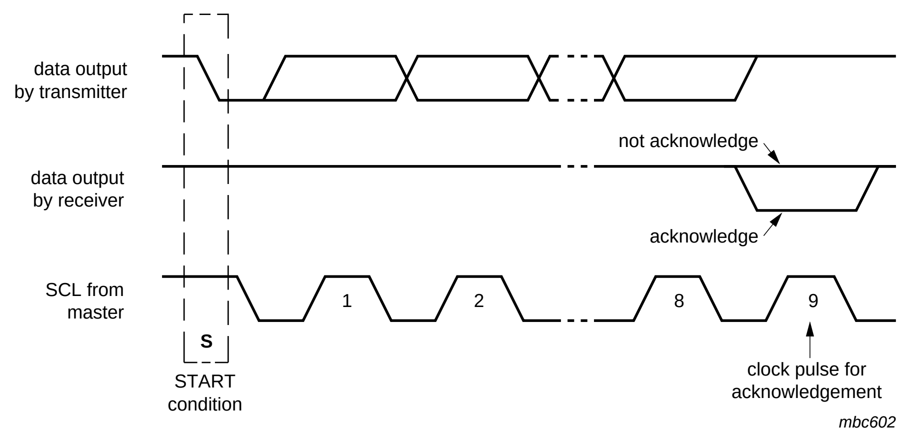


Fig 16. Acknowledgement on the I^{2}C-bus

9.5.7 Data transfer

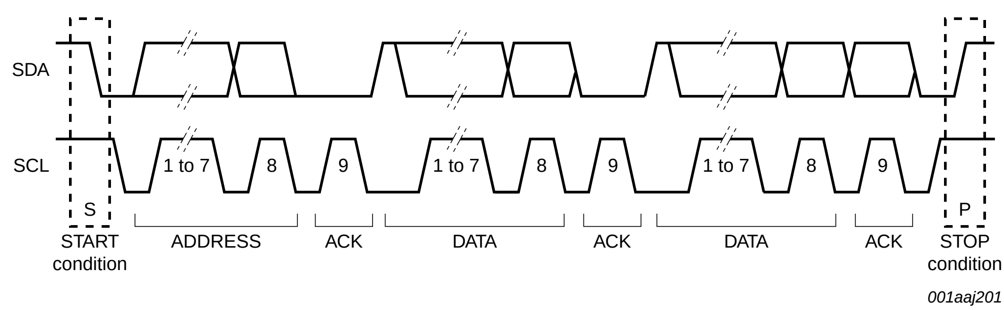


Fig 17. A complete data transfer

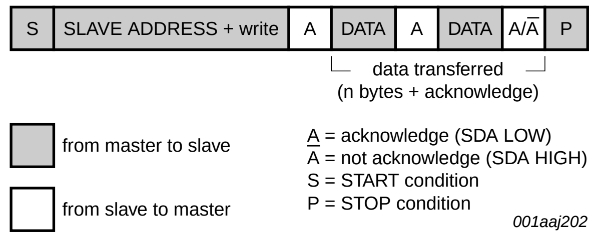


Fig 18. A master-transmitter addresses a slave receiver

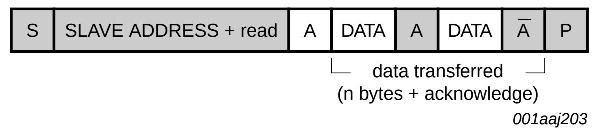
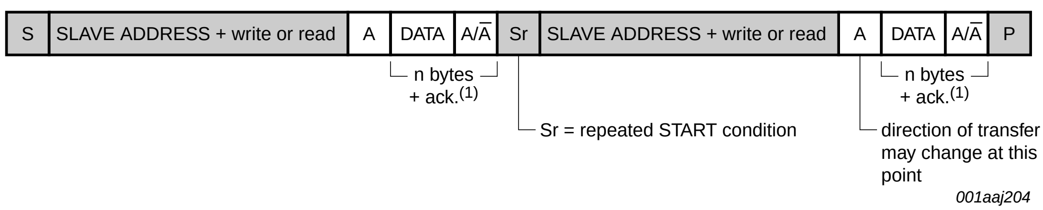


Fig 19. A master reads from a slave immediately after the first byte

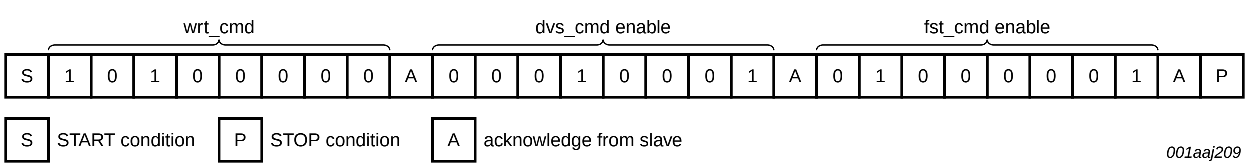


(1) Not shaded because transfer direction of data and acknowledge bits depends on R/W̄ bits.

Fig 20. Combined format

9.5.7.1 Example data transfers

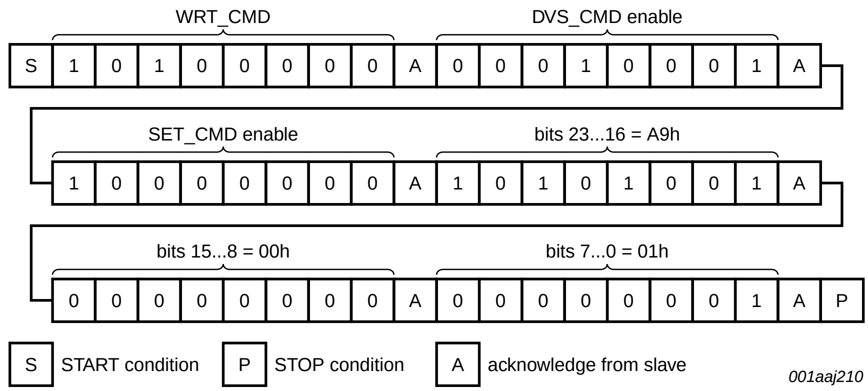
Example 1: Sending the instruction dvs_cmd followed by fst_cmd is shown in Figure 21.



Wrt_cmd is slave address plus write bit.

Fig 21. Sending instructions

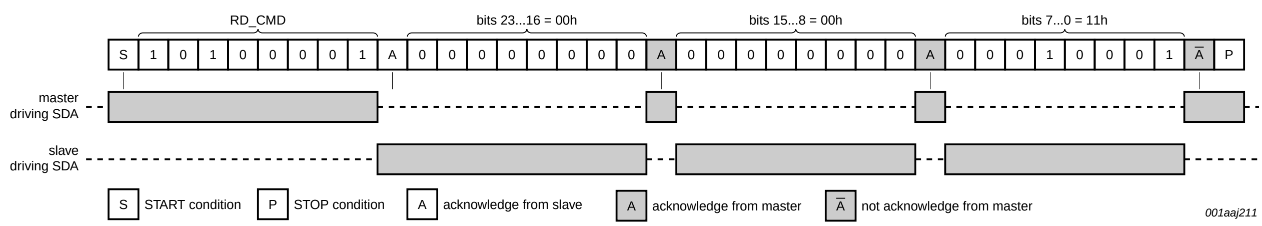
Example 2: Sending dvs_cmd followed by setting the counter to A90001h is shown in Figure 22



Wrt_cmd is slave address plus write bit.

Fig 22. Setting the counter

Example 3: Reading the counter (counter = 000011h) is shown in Figure 23.



Rd_cmd is slave address plus read bit.

Fig 23. Reading the counter

9.6 Instructions

9.6.1 Instruction set

Table 5. Write instructions

The writing protocol is illustrated in Figure 10.

First byte		Second byte		Further bytes	Action
Instruction	**Instruction code**	**Instruction**	**Instruction code**	**Parameters**	
wrt_cmd	1010 0000			-	device slave write address: slave address plus write bit
		dvs_cmd	0001 0001	-	stop and reset dividers
			0001 0000	-	start dividers
		pwd_cmd	0010 0001	-	shut down the device
			0010 0000	-	enable the device
		32k_cmd	0011 0001	-	enable output of 32.768 kHz on pin $\overline{\text{INT}}$
			0011 0000	-	disable output of 32.768 kHz on pin $\overline{\text{INT}}$
		fst_cmd	0100 0001	-	fast mode; increments counter every second
			0100 0000	-	fast mode disable
		set_cmd	1000 0000		set the counter value
				P1[23:16]	parameter with counter values
				P2[15:8]	
				P3[7:0]	

Table 6. Read instructions

The reading protocol is illustrated in Figure 11.

First byte		Further bytes	Action
Instruction	**Instruction code**	**Parameters**	
rd_cmd[1]	1010 0001		device slave read address: slave address plus read bit
		P1[23:16]	parameter with counter values; continues to read until no ACK is received; counter is not updated during this time
		P2[15:8]	
		P3[7:0]	
		P4[23:16]	
		:	

[1] Read of the counter is implicit with an interface read.

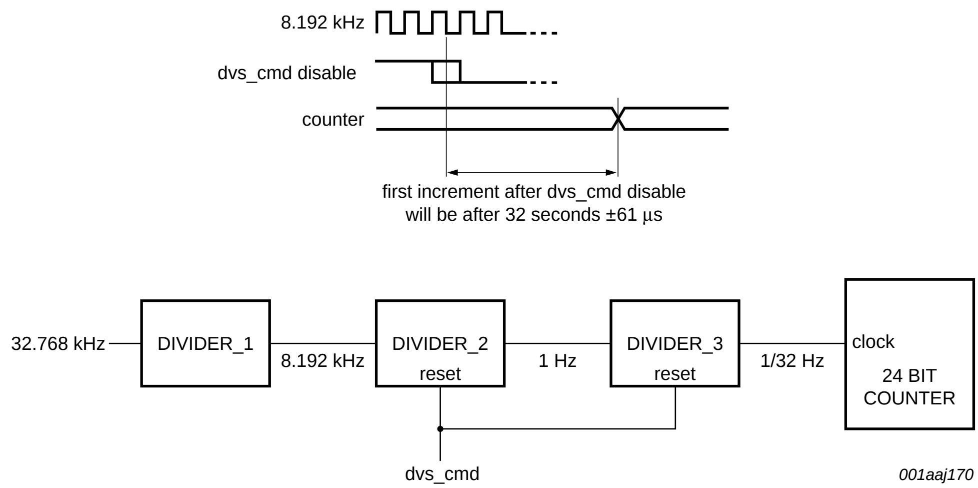
9.6.2 Instruction wrt_cmd

The write instruction (wrt_cmd) precedes each write sequence. Details of the writing protocol can be found in Section 9.5.1.1.

9.6.3 Instruction dvs_cmd

The divider switch instruction (dvs_cmd) can be used to freeze the divider chain and to put it in a defined state. The first two bits of the divider chain can not be influenced. With this instruction it is possible to control the time to the next increment of the counter. See Table 8.

When the dividers are restarted, the first increment of the 24 bit counter will be after 32 seconds.



Divider_1 = dividing by 4.

Divider_2 = dividing by 8192.

Divider_3 = dividing by 32.

Fig 24. Instruction dvs_cmd

When the dividers are restarted, the 8192 Hz clock could have just occurred and hence a delay of $^1/_{8192}$ seconds will occur before the next increment of the divider_2, or the 8192 Hz clock could be just about to occur and immediately increment the divider_2. As a consequence, an uncertainty of one half clock period will be present when restarting (see Figure 24).

9.6.4 Instruction pwd_cmd

The power down instruction (pwd_cmd) is intended to be used to put the system into a low power mode for storage. Static leakage current will be the only power consumed. Storage at temperatures above room temperature may increase leakage currents.

Entering power-down requires a specific sequence of events since under normal circumstances stopping the oscillator would result in a chip reset.

Table 7. Power-down sequence

Step	Action	Code sequence	Note
To enter power-down			
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	enable dvs_cmd	0001 0001	stop the divider
4	set counter with set_cmd	1000 0000	set the counter = AAAAAAh
		1010 1010	P1[23:16]
		1010 1010	P2[15:8]
		1010 1010	P3[7:0]
5	enable pwd_cmd	0010 0001	stop the oscillator
6	end transfer	STOP condition	-
7	device is now in a power-down state	-	-
To exit power-down			
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	disable pwd_cmd	0010 0000	oscillator starts on the ACK cycle of this instruction
4	disable dvs_cmd	0001 0000	enable the divider again
5	end transfer	STOP condition	-

9.6.5 Instruction 32k_cmd

The 32.768 kHz enable instruction (32k_cmd) is intended to aid with oscillator characterization during system development. With this instruction it is possible to obtain a 32.768 kHz clock on the $\overline{\text{INT}}$ pin which may be used for measurement.

This mode does not affect other operation of the chip with the exception of loss of interrupt output.

9.6.6 Instruction fst_cmd

The fast mode instruction (fst_cmd) is intended to enable faster system development. When enabled, the counter will increment once every second instead of once every 32 seconds. Interrupt pulses will also be generated once every second.

When using fst_cmd, data access to the device must be completed within 1 second, if not then counter increments will be lost. The 1 second period is measured from the ACK cycle of a valid slave address to the next STOP or repeated START. A repeated START will be sufficient to allow the counter to increment.

9.6.7 Instruction set_cmd

The counter can be set to any value using the set instruction (set_cmd). Partial writing of the data parameters will result in partial setting of the counter. E.g. if data transfer is stopped after P1[23:16] is transmitted, then only bit 23 to bit 16 will be updated.

This instruction takes only 3 parameters in one command. Data after the 3rd parameter will be interpreted as the next instruction.

Accurate setting and start-up can be implemented using the dvs_cmd instruction in cooperation with the set_cmd instruction. An example is shown in Table 8.

Table 8. Example of accurate setting of the counter

Step	Action	Code sequence	Note
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	enable dvs_cmd	0001 0001	-
4	set counter with set_cmd	1000 0000	set the counter = 1
		0000 0000	P1[23:16]
		0000 0000	P2[15:8]
		0000 0001	P3[7:0]
5	end transfer	STOP condition	-
6	wait for an external time marker	-	-
7	initiate transfer	START condition	-
8	send wrt_cmd	1010 0000	-
9	disable dvs_cmd	0001 0000	counter starts on the ACK cycle of this instruction
10	end transfer	STOP condition	-

9.6.8 Instruction rd_cmd

With the read instruction (rd_cmd) the counter value can be read at any time. When the counter value is read, the counter is frozen so that there will be no changes during the read back. After a read is terminated, the counter will be allowed to increment again. Any increment that was scheduled during the frozen period will then be effected.

Reading the counter is cyclic i.e. the device will repeatedly return the present counter value until the read is terminated. Reading the counter more than once may be useful in the case that the application is subject to a strong Electromagnetic Interference (EMI) environment so that read back values can be compared.

Read back must be terminated within 32 seconds else a count will be dropped.

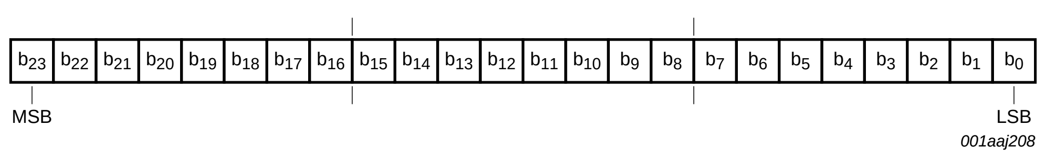


Fig 25. Read bit order

9.7 Reset

As described in Section 9.1, the device will be in reset when the oscillator is stopped with the exception of a controlled power-down using the pwd_cmd. The state of the device after reset is shown in Table 9.

Table 9. Reset state

Instruction name	State after reset
dvs_cmd	disabled
pwd_cmd	disabled
32k_cmd	disabled
fst_cmd	disabled
24 bit counter	000000h

10. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
I_{DD}	supply current			–50	+50	mA
V_I	input voltage			–0.5	+6.5	V
I_I	input current			–10	+10	mA
V_O	output voltage			–0.5	+6.5	V
I_O	output current			–10	+10	mA
P_{tot}	total power dissipation			-	300	mW
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	±2500	V
		MM	[2]	-	±200	V
I_{lu}	latch-up current		[3]	-	200	mA
T_{amb}	ambient temperature			–40	+85	°C
T_{stg}	storage temperature		[4]	–65	+150	°C

[1] Pass level; Human Body Model (HBM) according to JESD22-A114.

[2] Pass level; Machine Model (MM), according to JESD22-A115.

[3] Pass level; Latch-up testing, according to JESD78.

[4] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

11. Static characteristics

Table 11. Static characteristics

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = –40 °C to +85 °C; quartz crystal: R_s = 30 kΩ, C_L = 6.0 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		1.6	-	5.5	V
		T_{amb} = 25 °C; f_{SCL} = 0 Hz	-	1.0	-	V
ΔV_{DD}	supply voltage variation	$\Delta V/\Delta t$ = 1 V/µs	-	0.25	-	V
I_{DD}	supply current	power-down active [1]				
		T_{amb} = 25 °C; V_{DD} = 3 V; f_{SCL} = 0 Hz	-	3	-	nA
		device running				
		f_{SCL} = 0 Hz	-	-	400	nA
		T_{amb} = 25 °C; V_{DD} = 3 V; f_{SCL} = 0 Hz	-	130	-	nA
		interface active				
		f_{SCL} = 100 kHz	-	5	20	µA
		f_{SCL} = 1 MHz	-	50	100	µA
Oscillator						
V_{start}	start voltage		-	1.1	-	V
$t_{startup}$	start-up time		-	0.2	-	s
$C_{L(itg)}$	integrated load capacitance	[2]	-	6.0	-	pF
Inputs						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_I	input voltage	on pins SCL, OSCI, TEST	–0.5	-	5.5	V
		on pin SDA	–0.5	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}; on pins SCL, SDA and TEST	–200	0	+200	nA
Outputs						
V_O	output voltage		–0.5	-	V_{DD}+0.5	V
I_{OH}	HIGH-level output current	V_{OH} = 4.0 V; V_{DD} = 5 V; on pins $\overline{INT}$ and SDA	-	5	2	mA
		V_{OH} = 1.28 V; V_{DD} = 1.6 V; on pins $\overline{INT}$ and SDA	-	0.5	0.2	mA

Table 11. Static characteristics *…continued*

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = –40 °C to +85 °C; quartz crystal: R_s = 30 kΩ, C_L = 6.0 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 1.0 V; V_{DD} = 5 V; on pins $\overline{INT}$ and SDA	–2	–7	-	mA
		V_{OL} = 0.32 V; V_{DD} = 1.6 V; on pins $\overline{INT}$ and SDA	–0.4	–1	-	mA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}; on pins SDA and $\overline{INT}$	–200	0	+200	nA

[1] Unless otherwise defined, I_{DD} is measured with the reset state, see Section 9.7.

[2] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

12. Dynamic characteristics

Table 12. Dynamic characteristics

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing characteristics: serial bus						
f_{SCL}	SCL clock frequency		-	-	1	MHz
t_{LOW}	LOW period of the SCL clock		500	-	-	ns
t_{HIGH}	HIGH period of the SCL clock		260	-	-	ns
t_{BUF}	bus free time between a STOP and START condition		500	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		260	-	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		260	-	-	ns
t_r	rise time of both SDA and SCL signals	[2]	-	10	-	ns
t_f	fall time of both SDA and SCL signals	[2]	-	10	-	ns
$t_{SU;DAT}$	data set-up time		50	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		260	-	-	ns
$t_{VD;DAT}$	data valid time		75	-	450	ns
C_b	capacitive load for each bus line		-	-	50	pF
Timing characteristics: $\overline{INT}$						
$t_{w(int)}$	interrupt pulse width		20	40	80	µs

[1] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[2] Rise and fall times are not limited. Fast edges may lead to system EMI problems, whilst slow edges are susceptible to noise.

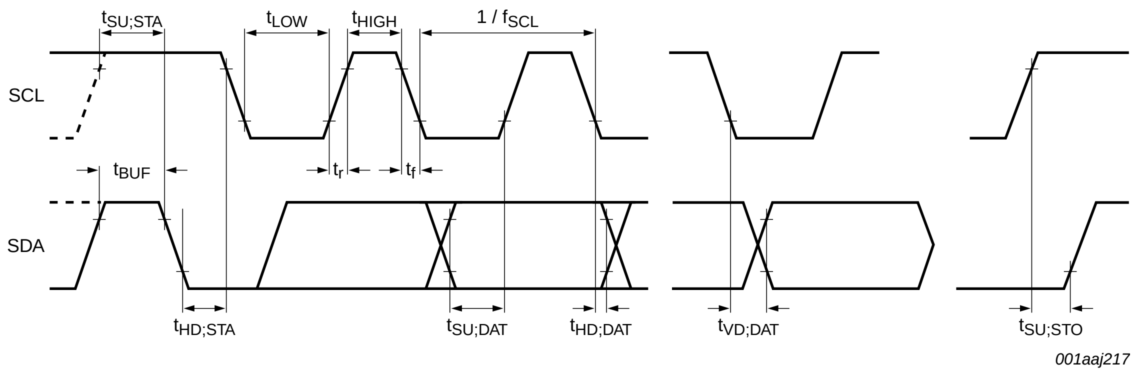


Fig 26. Serial bus timing waveforms

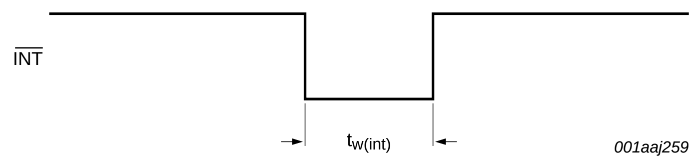


Fig 27. $\overline{INT}$ timing

13. Bare die information

13.1 Locations

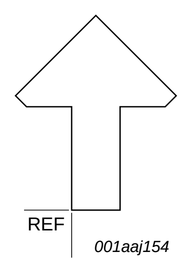
Table 13. Bump and reference point locations

Symbol	Pad	Coordinates[1]	
		x	y
$\overline{INT}$	1	437	–396
V_{DD}	2	–12	–430
TEST	3	–460	–396
OSCO	4	–460	1
OSCI	5	–460	396
V_{SS}[2]	6	–12	430
SCL	7	437	396
SDA	8	437	1
pin 1 identifier	-	474.7	–472.0
bottom left die corner[3]	-	–594.8	–568.2
top right die corner[3]	-	594.7	568.3

[1] All coordinates are referenced, in μm, to the center of the die (see Figure 30 and Figure 31).

[2] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically connected.

[3] Die size before dicing. Final dimensions will be 10 μm to 20 μm smaller.



Pin 1 is identified by this symbol.

Fig 28. Pin 1 identifier

13.2 PCB or foil landing site

The layout of the landing sites is important. It is recommended to follow the following guidelines

1. All landing sites should be the same size. When one site has a different size or shape, e.g. to indicate pad one, then the pull on the die produced by the surface tension of the solder will be different in one place. This variation can lead to the die not laying flat on the Printed-Circuit Board (PCB) or foil. This can also result in weak solder joints for some pins.
2. It is recommended to use circular landing sites of the same diameter as the solder ball. This will help with self alignment. Solder bump dimensions may be found in Figure 30.

3. If no solder resist is used on the PCB or foil, then consideration should be given to the amount of run-off of the solder along the track connected to the landing site. Uneven run-off may result in similar problems as described in 1.

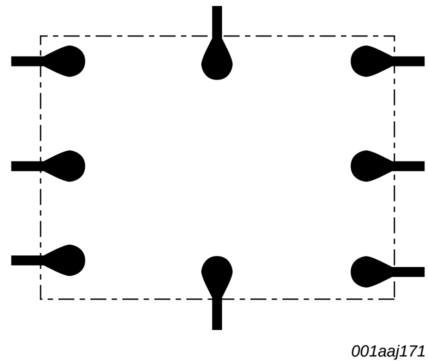
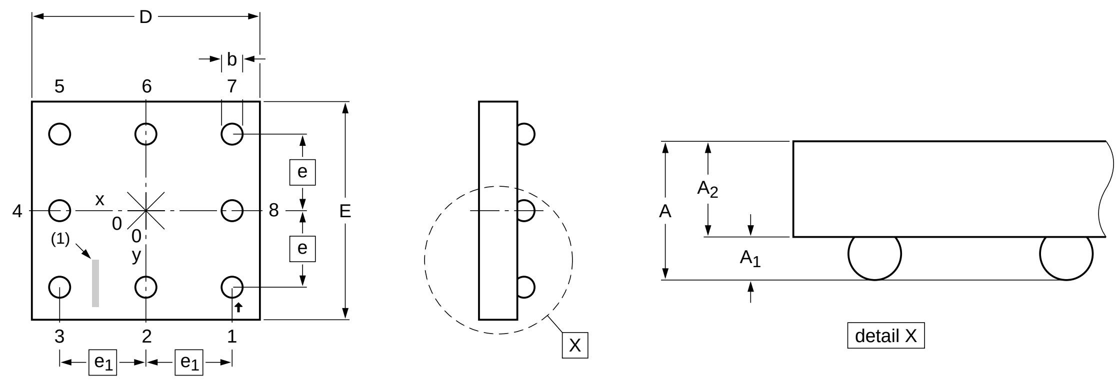


Fig 29. Example of PCB or foil landing sites

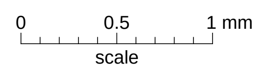
14. Bare die outline

WLCSP8: wafer level chip-size package; 8 bumps; 1.19 x 1.14 x 0.29 mm **PCA8802CX**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	e_1
mm	max		0.105		0.136				
	nom	0.29	0.090	0.2	0.109	1.19	1.14	0.4	0.45
	min		0.075		0.082				



Note

1. Marking code: PC8802-1.

pca8802cx_po

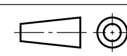
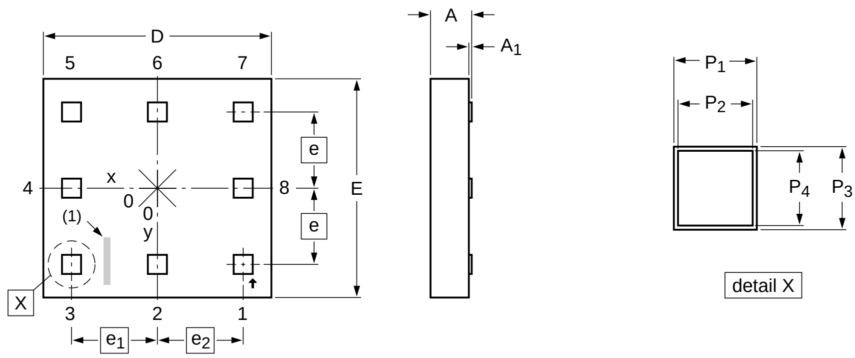
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA8802CX						08-11-28

Fig 30. Bare die outline PCA8802CX

WLCSP8: wafer level chip-size package; 8 bumps; 1.19 x 1.14 x 0.22 mm **PCA8802U**



Dimensions

Unit		A	A_1	D	E	e	e_1	e_2	$P_1^{(2)}$	$P_2^{(3)}$	$P_3^{(2)}$	$P_4^{(3)}$
	max		0.018							0.093		0.093
mm	nom	0.215	0.015	1.19	1.14	0.396	0.448	0.449	0.099	0.090	0.099	0.090
	min		0.012							0.087		0.087

Notes
1. Marking code: PC8802-1.
2. P_1 and P_3: pad size.
3. P_2 and P_4: bump size.

0 0.5 1 mm
scale

pca8802u_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA8802U						08-11-28

Fig 31. Bare die outline PCA8802U

15. Packing information

15.1 Tray information

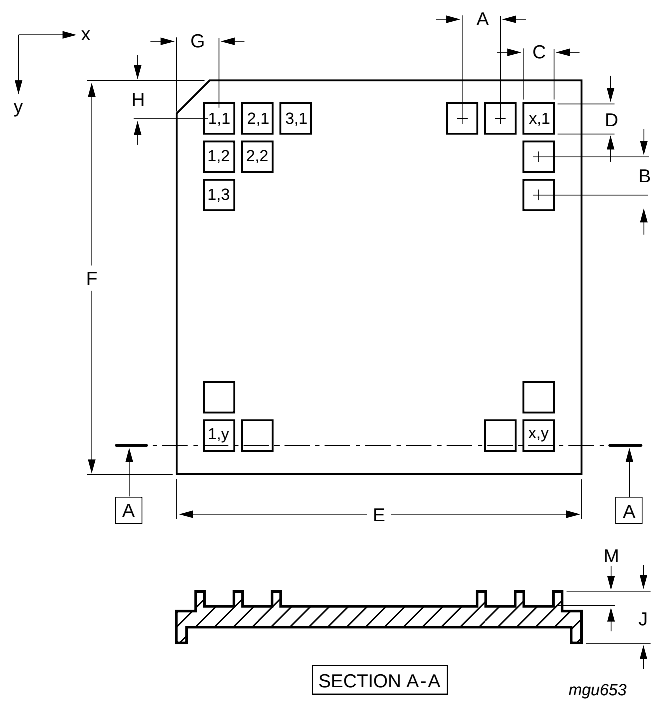
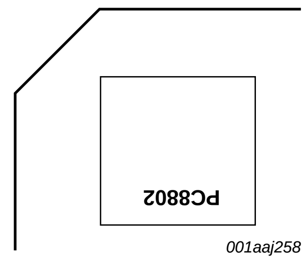


Fig 32. Tray details for PCA8802U

Table 14. Tray dimensions [1]

Dimension	Description	Value
A	pocket pitch; x direction	3.1 mm
B	pocket pitch; y direction	3.1 mm
C	pocket width; x direction	1.29 mm
D	pocket width; y direction	1.24 mm
E	tray width; x direction	50.8 mm
F	tray width; y direction	50.8 mm
G	distance from cut corner to pocket (1,1) center	5.25 mm
H	distance from cut corner to pocket (1,1) center	5.25 mm
J	tray thickness	3.96 mm
M	pocket depth	0.5 mm
x	number of pockets in x direction	14
y	number of pockets in y direction	14

[1] Die is placed in pocket bump side up.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the surface of the die, with respect to the cut corner on the upper left of the tray.

Fig 33. Tray alignment

15.2 Tape and reel

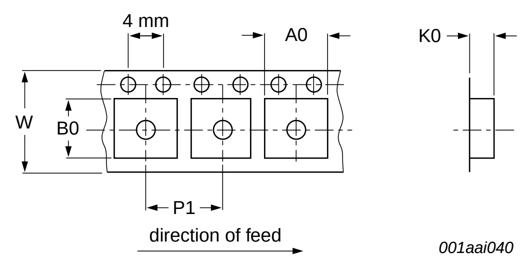
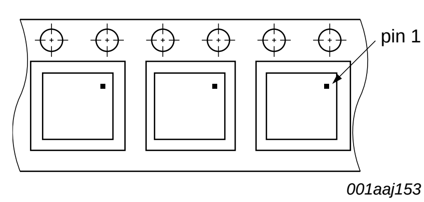


Fig 34. Tape and reel details for PCA8802CX

Table 15. Tape and reel dimensions [1]

Dimension	Description	Value
W	tape width	8.0 mm
A0	pocked length	1.3 mm
B0	pocket width	1.3 mm
K0	pocket depth	0.5 mm
P1	pocket pitch	4.0 mm

[1] Die is placed in pocket bump side down.



The orientation of the IC in a pocket is indicated by the position of pin 1, with respect to the sprocket holes.

Fig 35. Pocket alignment for PCA8802CX

15.3 Wafer and Film Frame Carrier (FFC) information

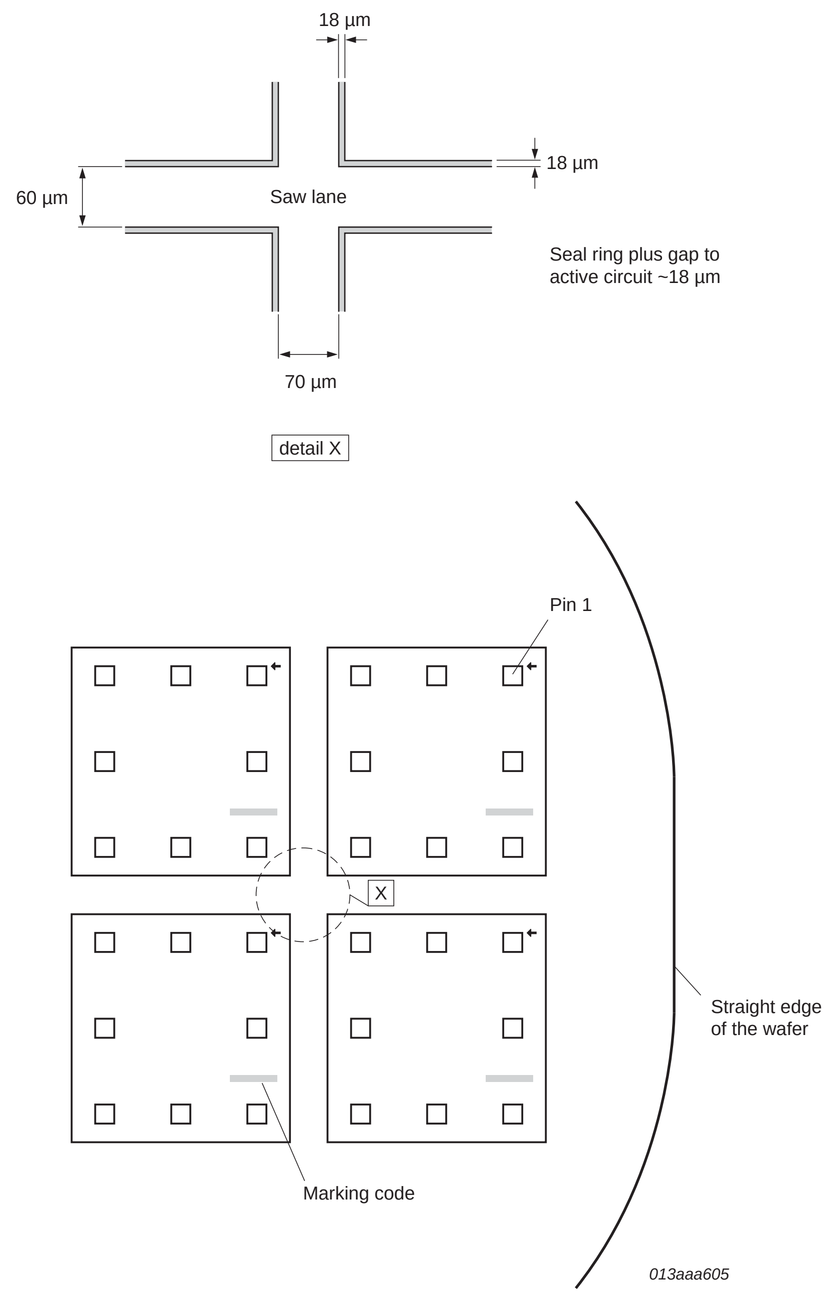


Fig 36. Wafer layout of PCA8802U/12AA/1

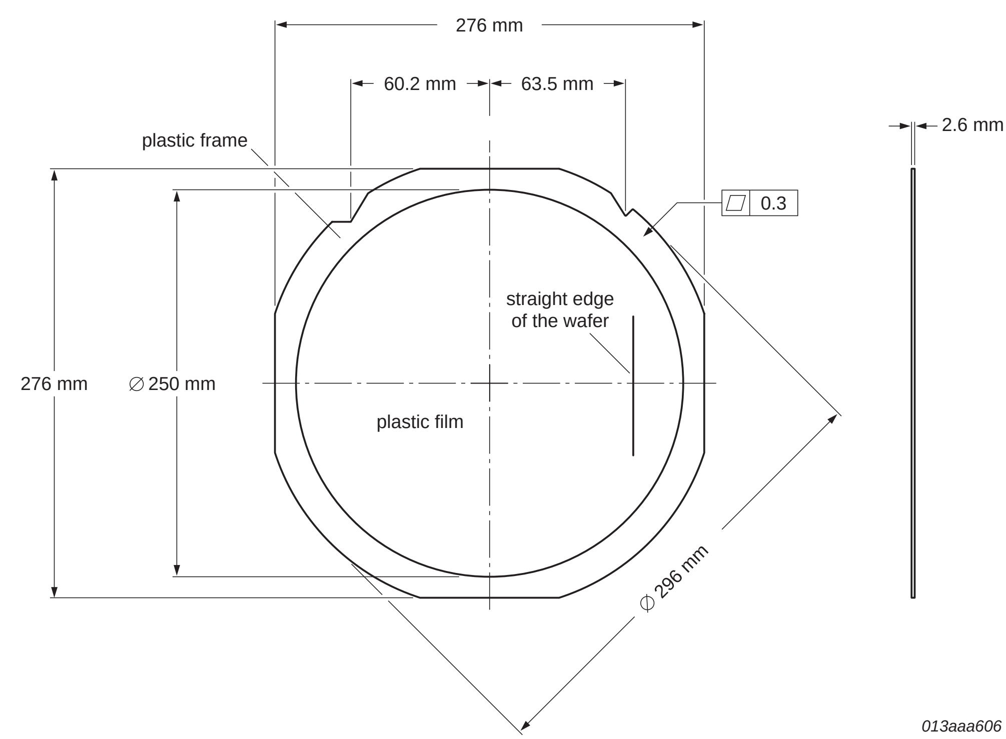


Fig 37. Film Frame Carrier (FFC) of PCA8802U/12AA/1

16. Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 “Wafer Level Chip Scale Package”* and in application note *AN10365 “Surface mount reflow soldering description”*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

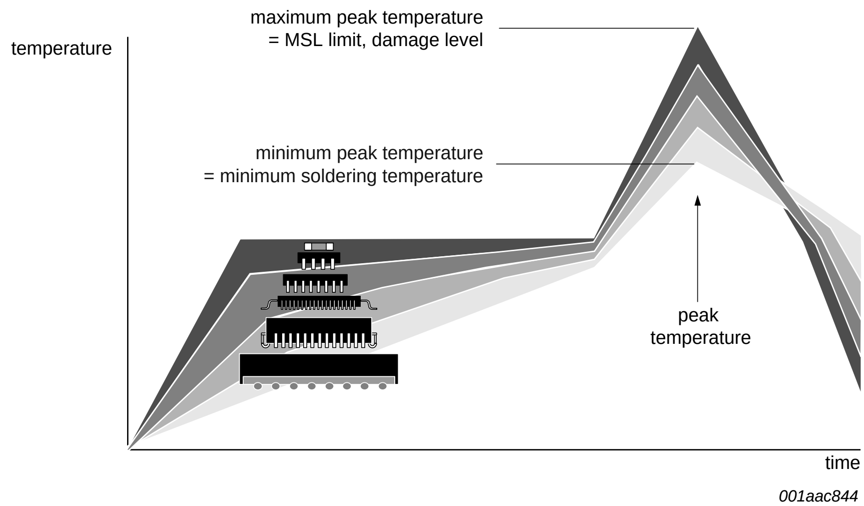
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 38) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16.

Table 16. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 38.



MSL: Moisture Sensitivity Level

Fig 38. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 “Surface mount reflow soldering description”*.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17. Abbreviations

Table 17. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EMI	ElectroMagnetic Interference
HBM	Human Body Model
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed-Circuit Board
RTC	Real Time Clock
WLCSP	Wafer Level Chip-Size Package

18. References

[1] **AN10439 —** Wafer Level Chip Size Package

[2] **AN10706 —** Handling bare die

[3] **AN10853 —** ESD and EMC sensitivity of IC

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **NX2-00001 —** NXP Semiconductors Quality and Reliability Specification

[11] **NX3-00092 —** NXP store and transport requirements

[12] **UM10204 —** I^2C-bus specification and user manual

19. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8802 v.3	20120330	Product data sheet	-	PCA8802 v.2
Modifications:	• Changed FFC information			
PCA8802 v.2	20120126	Product data sheet	-	PCA8802_1
PCA8802_1	20090219	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with NXP Semiconductors through its legal department.

20.4 Trademarks

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I²C-bus — logo is a trademark of NXP B.V.

21. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

22. Tables

23. Figures

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